REMARKS

In the above-identified office action the Examiner has rejected claims 2, 3 and 7 under 35 U.S.C. § 112. These claims have been cancelled thereby obviating this rejection. In addition, claim 7 has been rejected under 35 U.S.C. § 102(b) as anticipated by Shimanuki et al. Applicant has cancelled claim 7 as well, thereby obviating this rejection.

Claims 3-5 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Iida et al. Claims 3-5 have also been cancelled thereby obviating this matter.

Further, claims 3-5 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Hourai et al. As stated above, claims 3-5 have been cancelled. Accordingly, this rejection is considered obviated. Claims 2 and 4-5 have been rejected as unpatentable over Iida et al. or Hourai et al. in view of Shimanuki et al. These claims have also been cancelled. Accordingly, this rejection is considered obviated. Claim 7 has been rejected as being over Kim et al. in view of Luter et al. Claim 7 has been cancelled and accordingly, this rejection is considered obviated.

Claims 9-13 have been rejected as being unpatentable over Adachi et al. in view of Iida et al. The Examiner stated that Adachi's preferred annealing conditions is to ramp up to a temperature in excess of 1100°C with annealing performed at temperatures ranging from 500°C to 900°C for more than ten minutes. The Examiner has also stated Iida teaches a method of forming a single crystal wafer with very few crystal defects. Accordingly, the Examiner would modify Adachi et al. with Iida et al.'s silicon wafer to form a uniform precipitation.

The Examiner admits that the combination of Adachi et al. and Iida et al. does not teach a heat temperature at the initial entry of the silicone single crystal wafer to be a target of the heat treatment is 500°C or less. The Examiner concludes that it would have been obvious to modify Adachi by attempting to optimize same by conducting routine experimentation.

Applicant has amended claims 9, 10 and 11 so that they now reflect that the heat treating method of the subject invention maintains the heat treatment temperature at the initial entry of the silicone single crystal wafer to be less than 500°C while maintaining a temperature ramping rate with an ultimate temperature in the range of 700°C to 900°C with a ramping rate of 1°C per minute or less. This is not shown in the art.

Adachi teaches a maximum temperature of 1380°C (Col. 7, line 5), and throughout his specification the practice of annealing the wafers in temperatures of excess of 1100°C (Col. 9, line 3); further that the preferred annealing conditions for forming a defect free region (DZ layer) is to ramp up to a temperature in excess of 1100°C (Col. 10, lines 60-62). Multiple other instances abound in Adachi's specification concerning temperatures maintaining temperatures above 1100°C. Applicant has amended claims 9 and 10 so that now the heat treatment temperature is maintained in a range of 700°C to 900°C, substantially below Adachi's temperatures. Thus, while Adachi may teach annealing at temperatures from 500°C to 900°C, this is after heating it at temperatures in excess of 1100°C; thus Adachi is not maintaining the temperature at 500°C, but rather having a maximum temperature of 1100°C or more and then down to 500°C to 900°C. This is different than as now claimed. As such, claims now recite over the combination of Adachi and Iida.

The inventions of claims 9-13 are to make uniform the oxide precipitates in a silicon wafer prepared by controlling the parameters of the time when heat-treating the wafer. On the other hand, the technique of Adachi et al. (US 5,931,662) is to simply generate oxide precipitates in a silicon wafer by controlling the parameters of the time when heat treating the wafer (Col. 1, lines 17-20). Adachi does not discuss the uniformity of oxide precipitates at all.

Since the present invention and the technique of Adachi are different in the "respective objectives", the parameters to be controlled and the ranges thereof are different. Claims 9-13 recite the parameters required for making uniform the oxide precipitates and their numerical ranges, of the basis for which is shown in the Table B1 of the present application. According to Table B 1, it is noted that the oxide precipitates are not made uniform in a part of the range of the parameters described in Adachi (Col. 10, line 65 through Col. 11, line 4). This means that the technique of Adachi is fundamentally different from the present invention.

The technique of Iida et al. (US 5,968,264) is to make the distribution of oxygen concentration of a single crystal to be a predetermined level or less by controlling the parameters of the time when pulling up the single crystal (Col. 13, lines 60-67). Iida improves the uniformity of the oxide precipitates by heat-treating the wafer. However, in Iida, it is assumed that a single crystal having the oxygen concentration distribution of a predetermined value or less is generated and wafers are cutout from that single crystal (Col. 14, lines 1-12). In other words,

the uniformity of the oxide precipitates by Iida is not caused by the control at the time when heat-treating the wafer, but caused by the control at the time when pulling up the single crystal. Therefore, the technique of Iida is completely irrelevant to the present invention in which the oxide precipitates are made uniform by controlling the parameters of the time when heat-treating the wafer.

As stated above, none of the cited references describe the connection between the control of the parameters of the time when heat-treating the wafer and the uniformity of the oxide precipitates in the silicon wafer. Therefore, it is impossible to arrive at the present invention (in which the oxide precipitates in the silicon wafer are made uniform by controlling the parameters of the time when heat-treating the wafer), by the combination of the technique of Adachi which simply generates the oxide precipitates and the technique of Iida which simply makes the oxide precipitates to be a predetermined value or less.

Applicants hereby request reconsideration and reexamination thereof.

With the above amendments and remarks, this application is considered ready for allowance and Applicants earnestly solicit an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

Respectfully submitted,

WELSH & KATZ, LTD.

Gerald T. Shekleton
Registration No. 27,466

Date: April 5, 2004
WELSH & KATZ, LTD.
120 South Riverside Plaza
22nd Floor
Chicago, Illinois 60606-3913
Telephone: 312/655-1500